Materials Science in Electronics devices
- Semiconductor devices -

2016 Yutaka Oyama
oyama@material.tohoku.ac.jp
http://www.material.tohoku.ac.jp/~denko/lab.html

Contents

半導体デバイスは、「**金属・半導体・セラミックス**」を総合して形成。
理想型静電誘導トランジスタのプロセス例

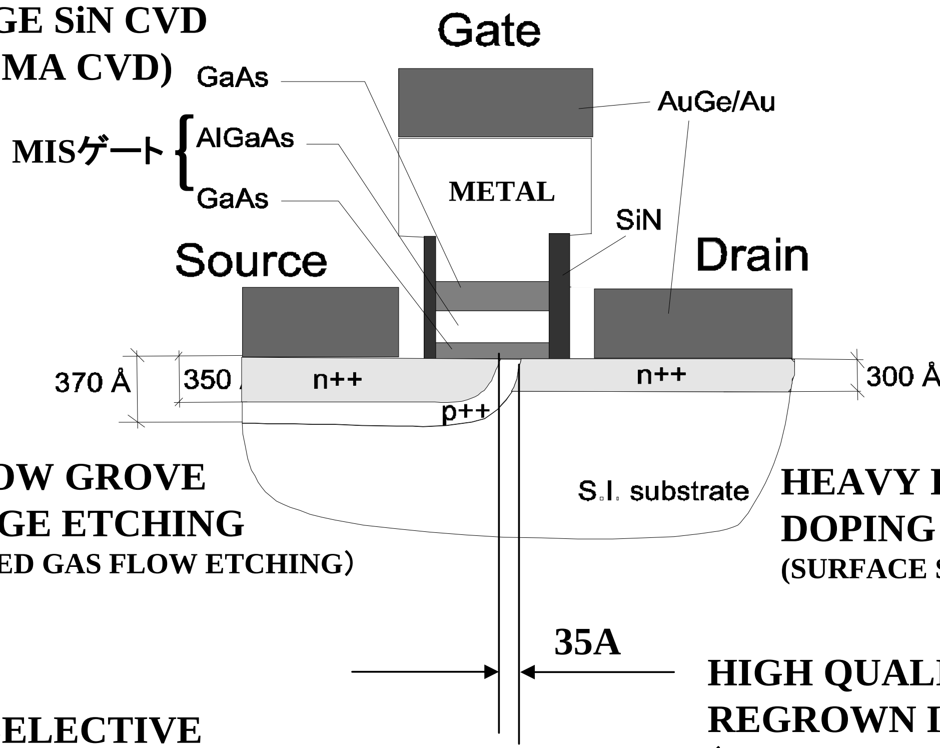
DETAILED CRITICAL PROCESSES FOR ISIT

METAL/CERAMICS/SEMICONDUCTOR BREAKTHROUGH PROCESSES

SELECTIVE EPITAXY
（SELF-ALIGN PROCESS）

LOW ρ_c CONTACT（METAL/SEMI CONTACT）
NON-ALLOYED
VERY THIN MIXED LAYER

LOW-T&DAMAGE SiN CVD
（REMOTE PLASMA CVD)

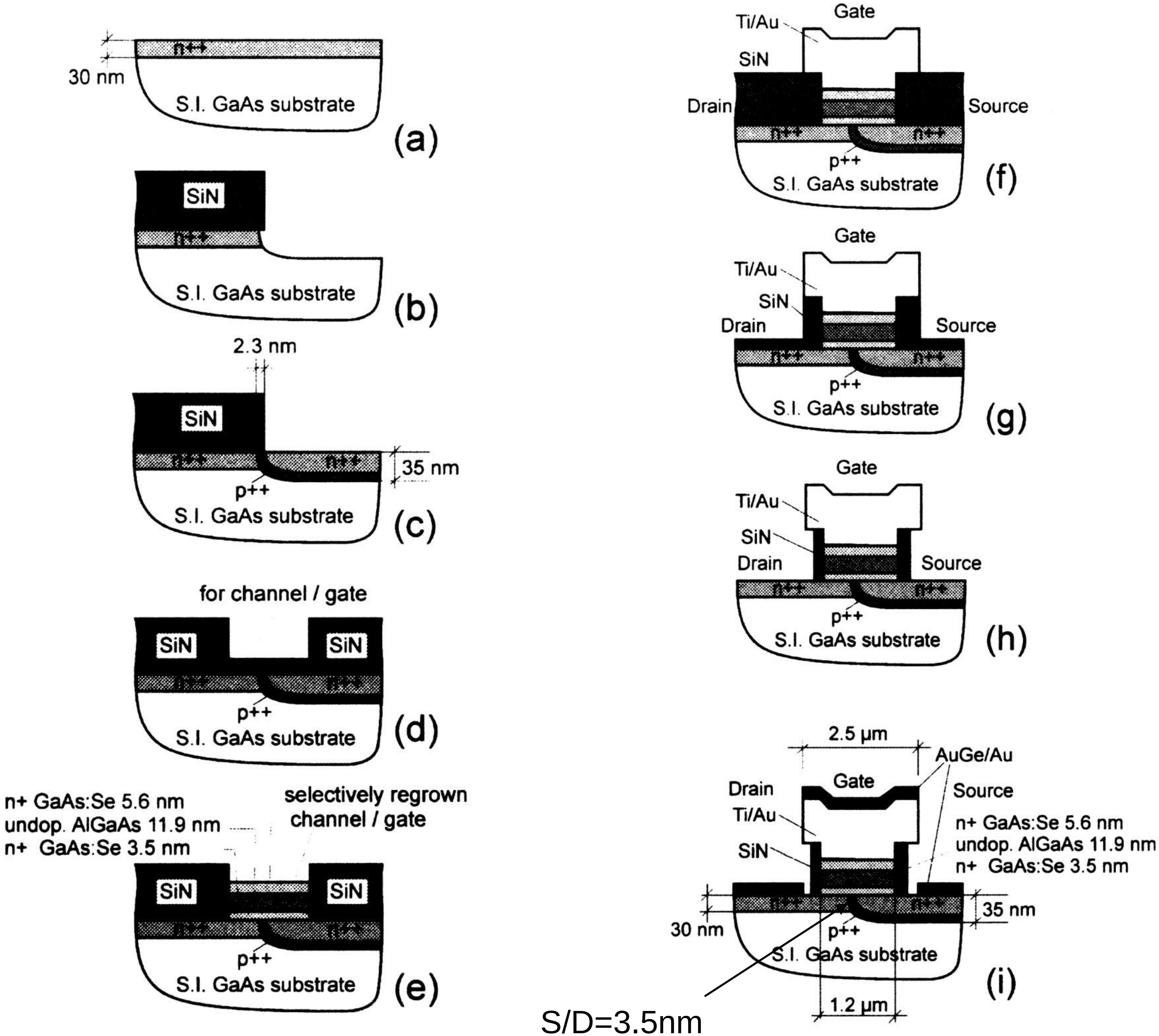


ULTRA SHALLOW GROVE
LOW-T&DAMAGE ETCHING
（PHOTO-STIMULATED GAS FLOW ETCHING）

HEAVY DOPING
DOPING EPITAXY 10^{19}-10^{20}cm^{-3}
(SURFACE STOICHIOMETRY CONTROL)

HIGH QUALITY
REGROWN INTERFACE
（SURFACE STOICHIOMETRY CONTROL）

LOW-T& SELECTIVE
MOLECULAR LAYER EPITAXY (MLE)
WITH ATOMIC ACCURACY (AA)


n++
30 nm
S.I. GaAs substrate
(a)
SiN
n++
S.I. GaAs substrate
(b)
2.3 nm
SiN
n++
n++
35 nm
p++
S.I. GaAs substrate
(c)
for channel / gate
SiN
SiN
n++
n++
p++
S.I. GaAs substrate
(d)
n+ GaAs:Se 5.6 nm
undop. AlGaAs 11.9 nm
n+ GaAs:Se 3.5 nm
selectively regrown
channel / gate
SiN
SiN
n++
n++
p++
S.I. GaAs substrate
(e)
Gate
Ti/Au
SiN
Drain
Source
n++
n++
p++
S.I. GaAs substrate
(f)
Gate
Ti/Au
SiN
Drain
Source
n++
n++
p++
S.I. GaAs substrate
(g)
Gate
Ti/Au
SiN
Drain
Source
n++
n++
p++
S.I. GaAs substrate
(h)
2.5 μm
AuGe/Au
Drain
Gate
Source
Ti/Au
n+ GaAs:Se 5.6 nm
undop. AlGaAs 11.9 nm
SiN
n+ GaAs:Se 3.5 nm
n++
n++
35 nm
30 nm
p++
S.I. GaAs substrate
(i)
1.2 μm
S/D=3.5nm

薄膜ｴﾋﾟﾀｷｼｬﾙ成長　Thin film epitaxial growth

□液相ｴﾋﾟﾀｷｼ

LPE
Liquid phase epitaxy

希薄環境相の結晶成長
徐冷法
ﾈﾙｿﾝ法
温度差法

LED,LDなど
発光ﾃﾞﾊﾞｲｽの大量生産
一般的にはﾐｸﾛﾝ･ｻﾌﾞﾐｸﾛﾝﾃﾞﾊﾞｲｽに適用
高純度（偏析効果）･高品質
低コスト

□気相ｴﾋﾟﾀｷｼ

VPE
Vapor phase epitaxy

塩化物気相ｴﾋﾟﾀｷｼ
有機金属気相ｴﾋﾟﾀｷｼ（MOVPE)
など

発光ﾃﾞﾊﾞｲｽ～ﾄﾗﾝｼﾞｽﾀ･量子効果ﾃﾞﾊﾞｲｽまで
ﾐｸﾛﾝ～ｻﾌﾞﾐｸﾛﾝ～ナノ構造まで広範囲
原料の高純度化
気相反応＋表面反応

□超高真空ｴﾋﾟﾀｷｼ

UHV
Ultra high vacuum epitaxy

分子線ｴﾋﾟﾀｷｼ(MBE)
分子層ｴﾋﾟﾀｷｼ（MLE,ALE)
ｹﾐｶﾙﾋﾞｰﾑｴﾋﾟﾀｷｼ（CBE)
など

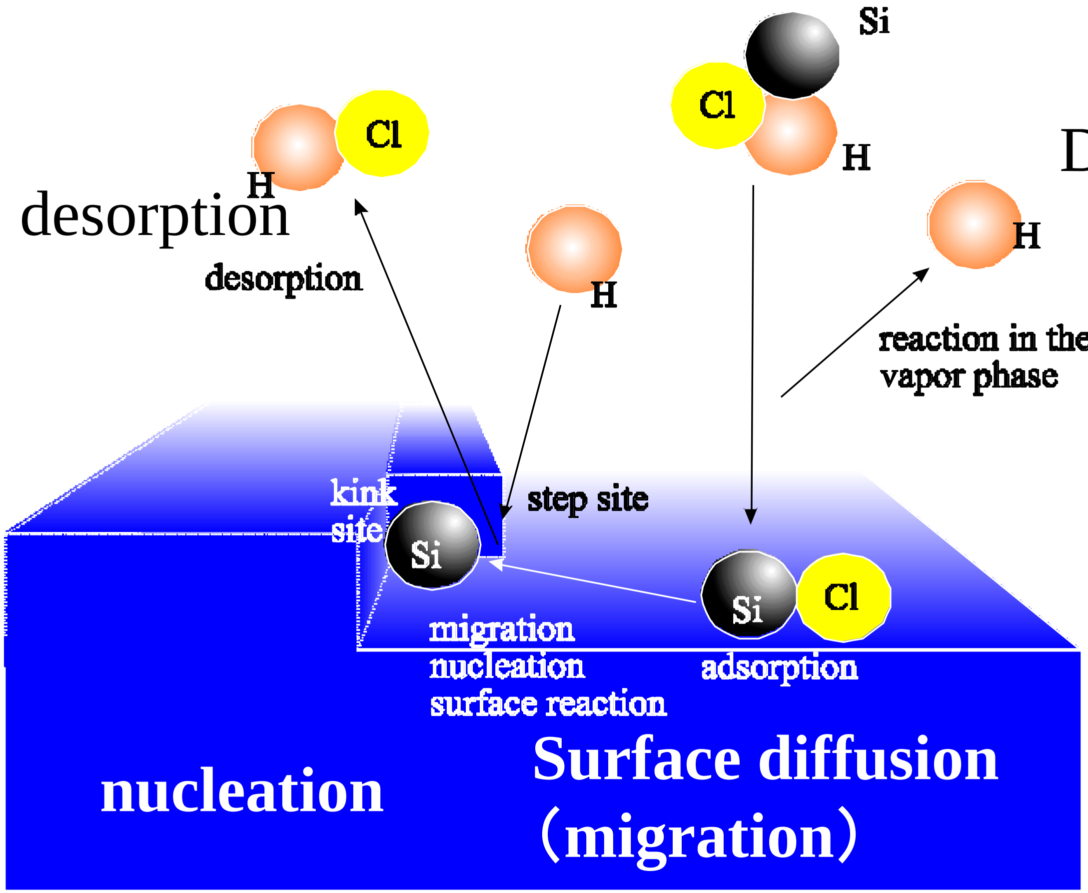
発光ﾃﾞﾊﾞｲｽ～ﾄﾗﾝｼﾞｽﾀ･量子効果ﾃﾞﾊﾞｲｽまで
ﾐｸﾛﾝ～ｻﾌﾞﾐｸﾛﾝ～ナノ構造まで広範囲
原料の高純度化
表面反応

Detailed reaction processes of Epitaxial growth

Vapor phase or solution reaction

Diffusion to the surface

desorption



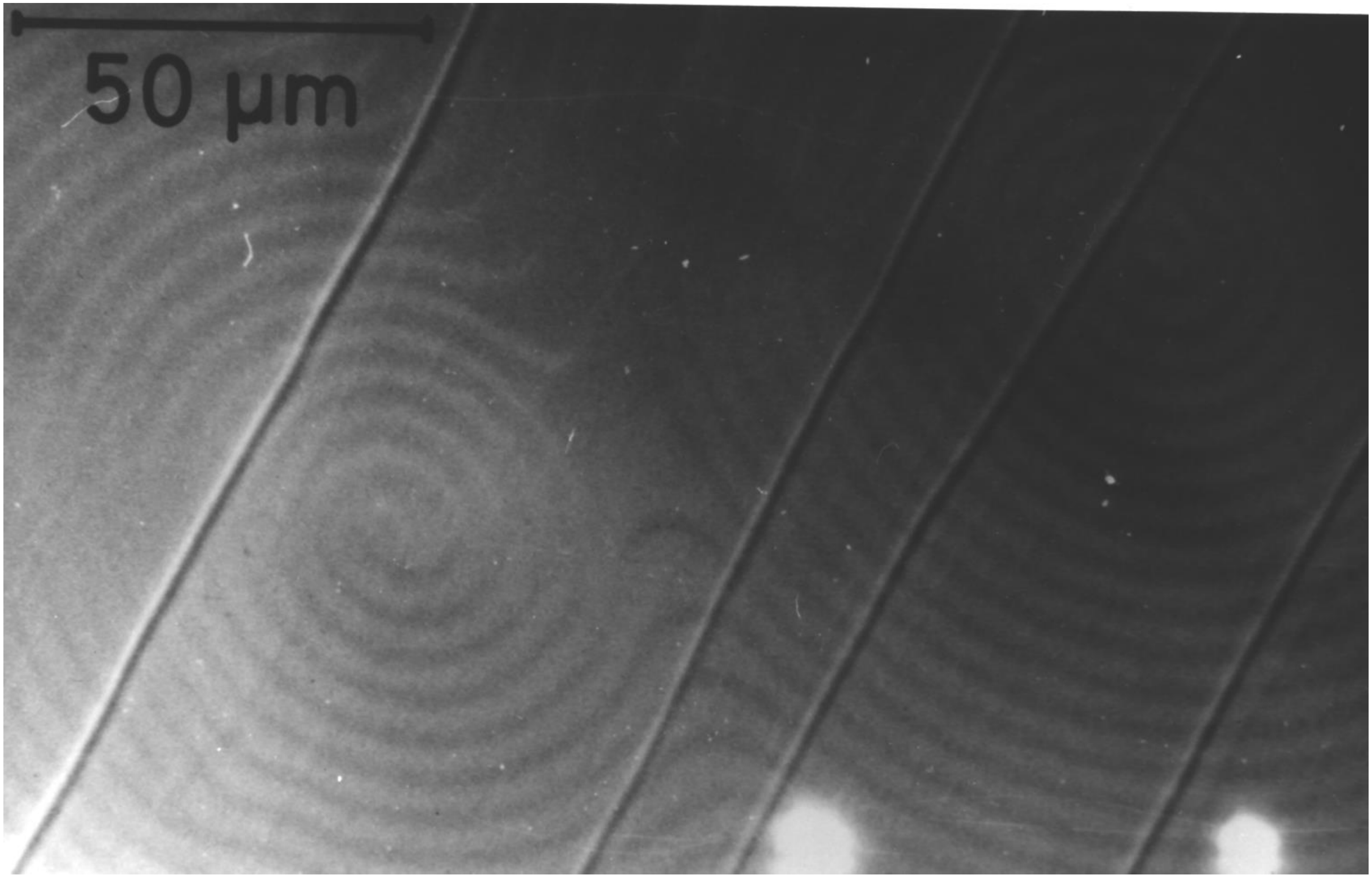
Surface adsorption

Surface reaction

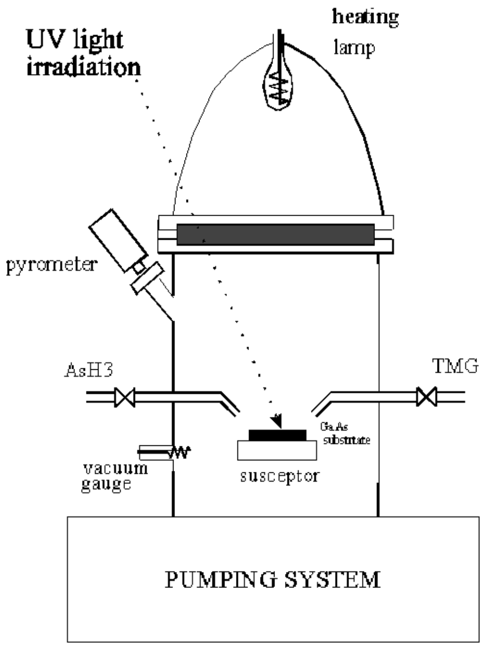
Real surface reaction
process in MLE Si

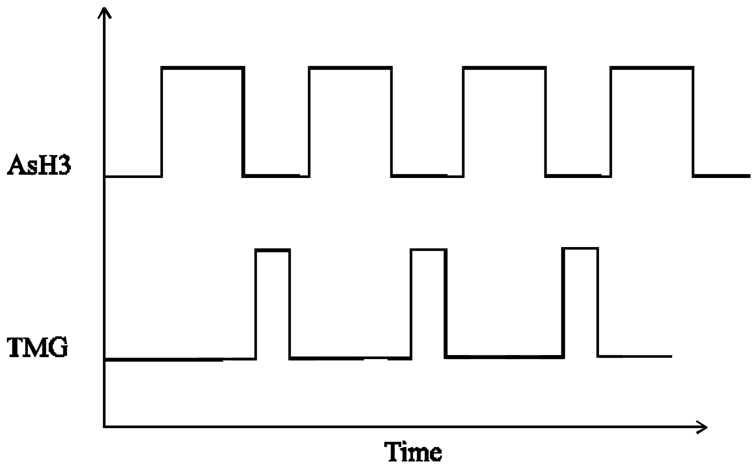
Si_react

Spiral growth necleus centers on facets
LPE GaAs (screw dislocation)



Principle of MLE :GaAs case





✧**Molecular Layer Epitaxy in brief**

ALE(Atomic Layer Epitaxy) of poly-ZnS on glass substrate for EL application

T. Suntola, U.S. Patent 4058430, 1977.

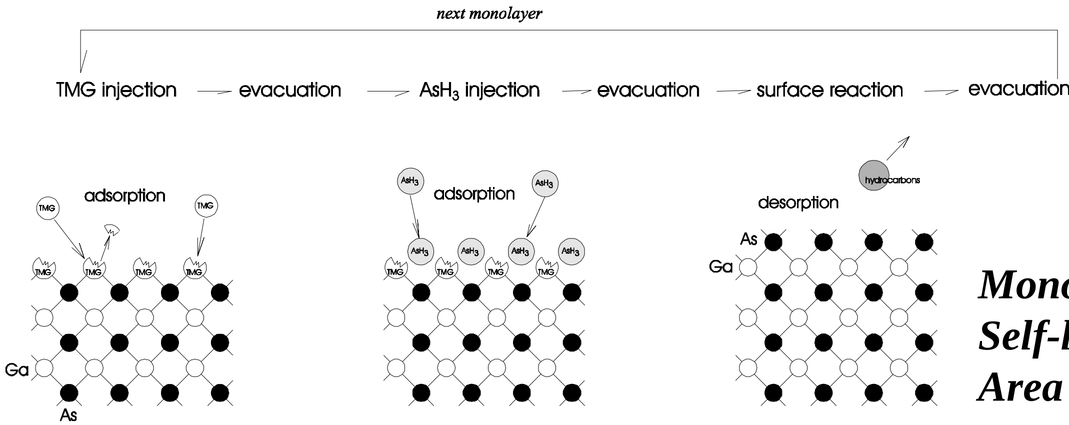
M. Ahonen, M. Pessa, T. Suntola, Thin Solid Films <u>65</u> (1980) 301.

MLE(Molecular Layer Epitaxy) of GaAs single crystal on GaAs

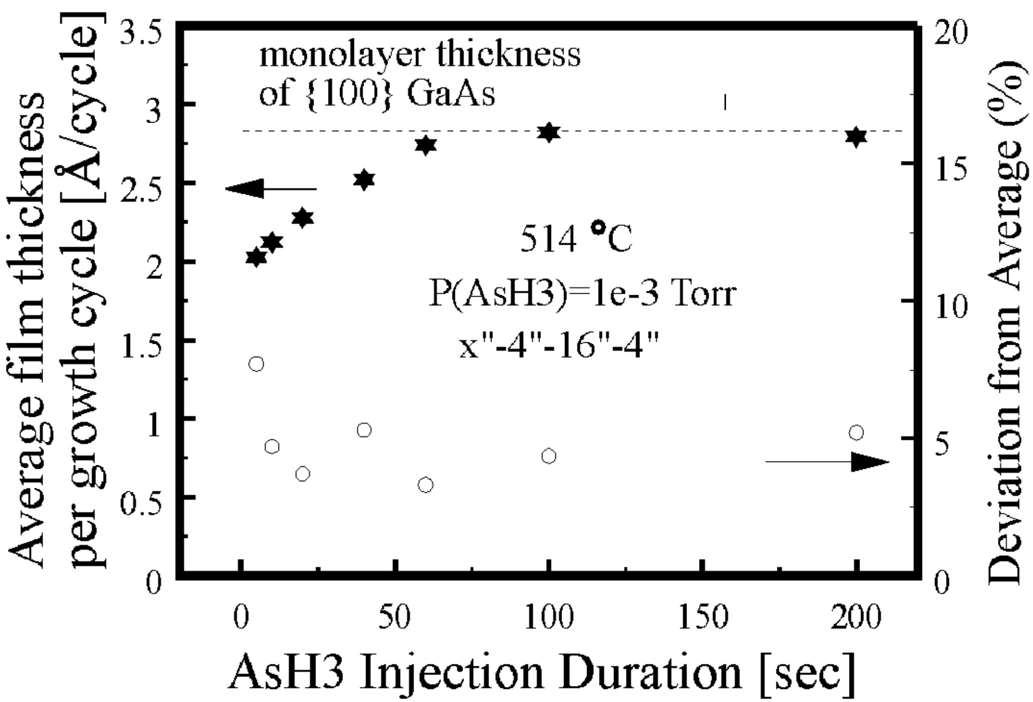
J. Nishizawa et. al. Extended Abstracts of the 16th Conference on Solid State Device and Materials (The Japan Society of Applied Physics, Kobe, Japan, 1984), p. 1.

J. Nishizawa, et. al. J. Electrochem. Soc., <u>132</u> (1985) 1197.

Principle of MLE



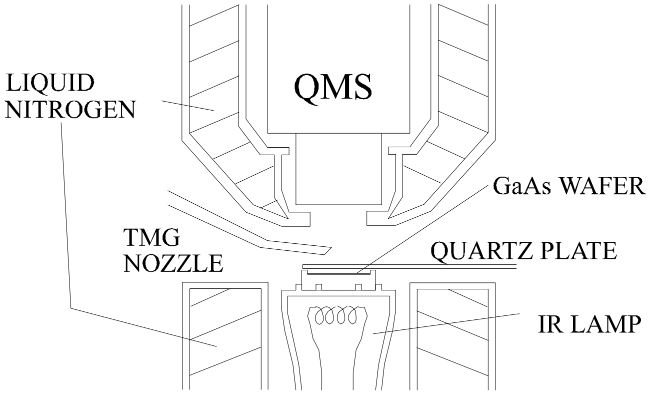
Mono-molecular layer epitaxy
Self-limiting epitaxy with atomic accuracy (AA)
Area selective epitaxy



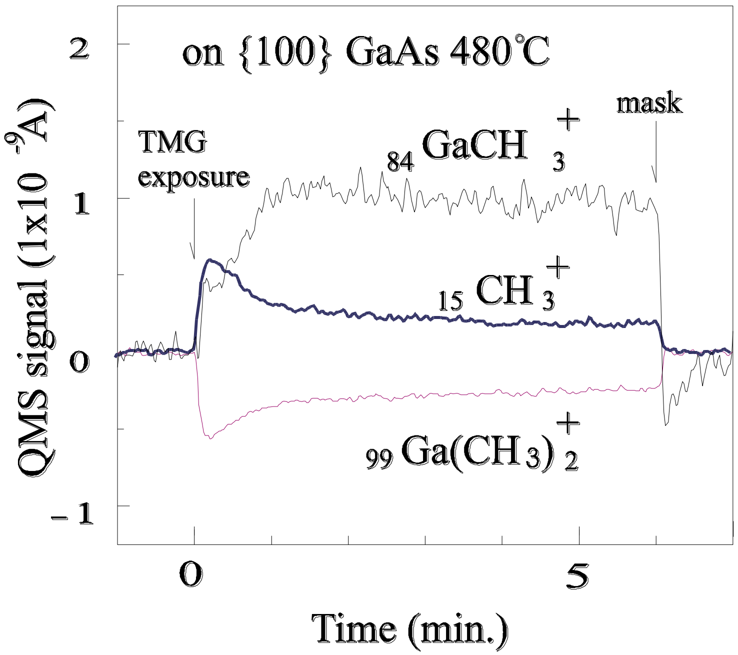
Molecular layer epitaxy of GaAs
Thin Solid Films, 225 (1993), 1-6.
Jun-ichi Nishizawa, Hiroshi Sakuraba Yutaka Oyama など

Surface reaction process

investigation of surface reaction paths of
molecular layer epitaxy with
quadrupole mass spectrometer



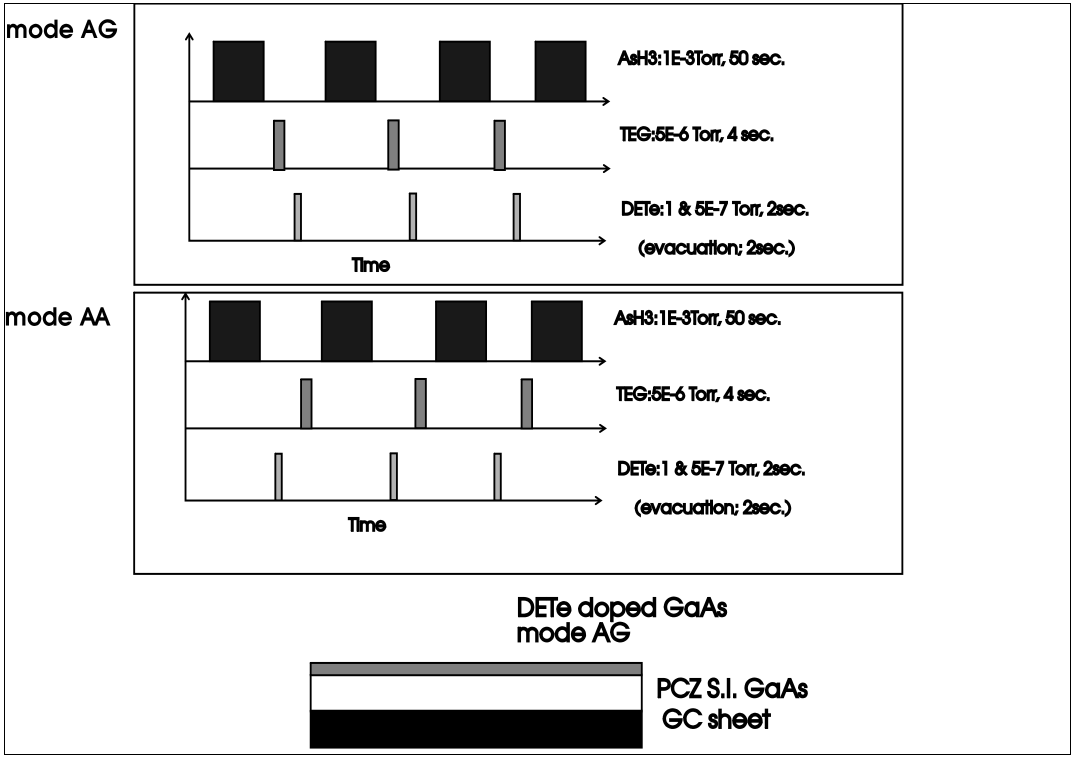
Experimental setup.
Quartz plate is moved to expose or
mask GaAs wafer

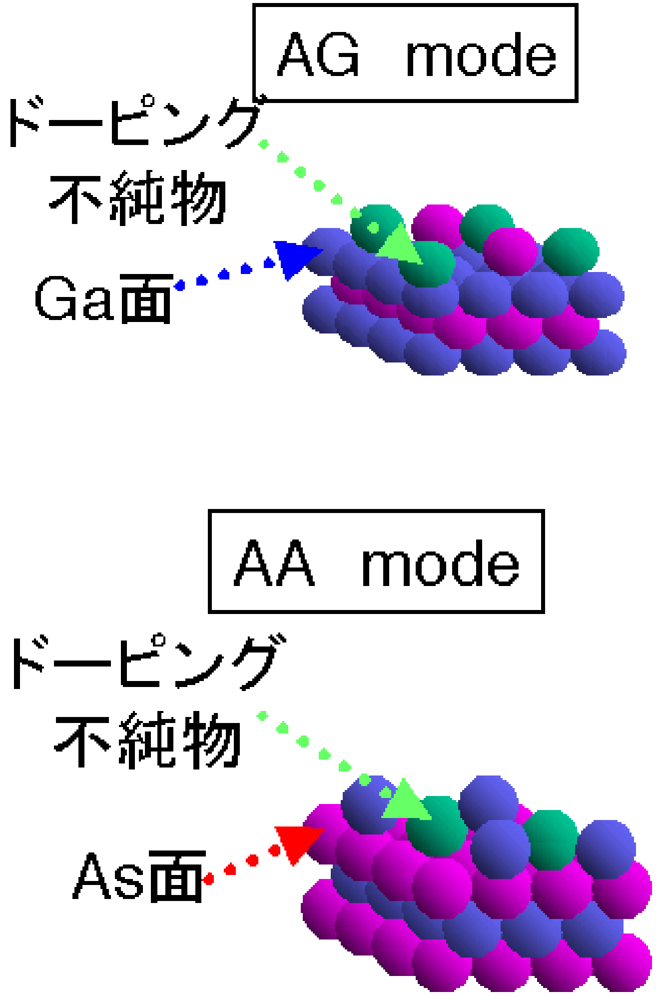


QMS signals measured on {100} n+ GaAs substrate.

file: qms_100

Impurity doping: control of surface stoichiometry

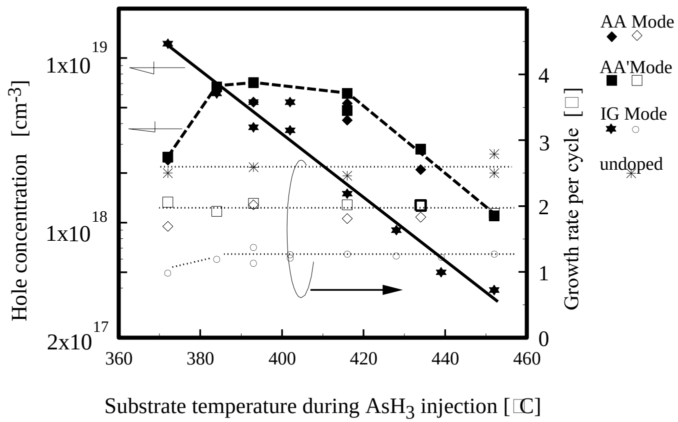




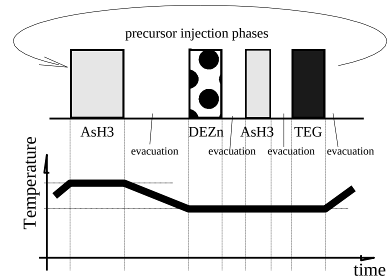
Electrical activation of Te and Se in GaAs at extremely heavy doping up to 5 × 1020cm-3 prepared by intermittent injection of TEG/AsH3 in ultra-high vacuum,
Journal of Crystal Growth, Volume 212, Issues 3-4, May 2000, Pages 402-410
Yutaka Oyama, Jun-ichi Nishizawa, Kohichi Seo and Ken Suto など

Ohno T et. al.

DOPING CHARACTERISTICS OF p-GaAs:Zn MLE

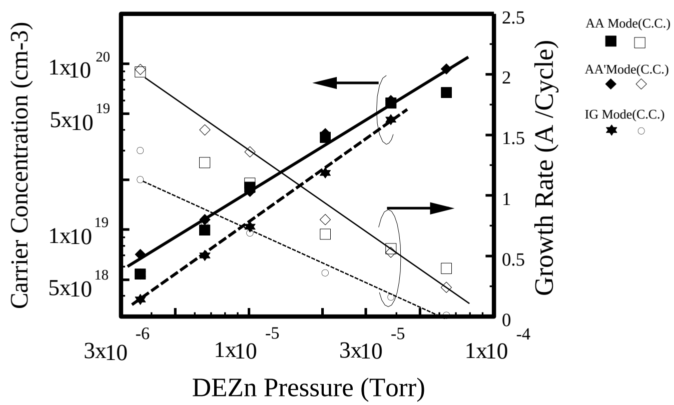


Growth rate and hole concentration vs. temperature during arsine injection for Zn doped GaAs grown with temperature synchronized MLE.



temperature synchronized molecular layer epitaxy

AA' - after arsine doping mode

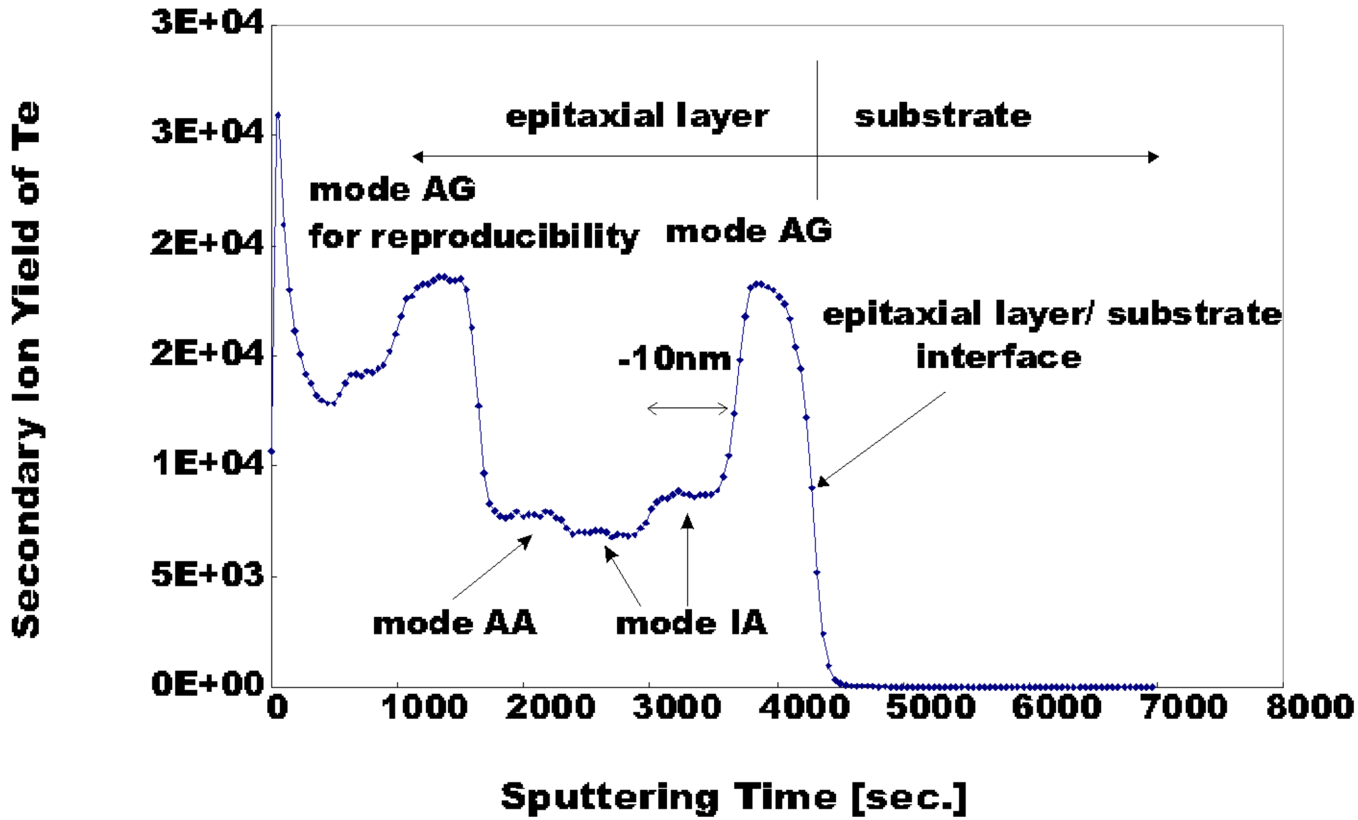


Hole concentration vs. DEZn pressure for Zn doping for temperature synchronized MLE.

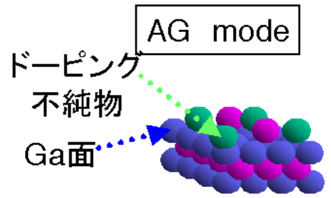
Zinc doping of GaAs grown with temperature synchronized molecular layer epitaxy

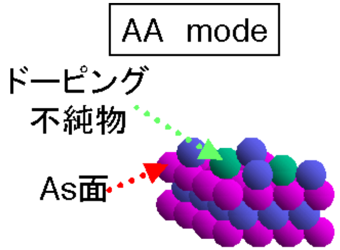
file: d:\0q\fig_s56s.cdr
ZnTS.cdr

Extremely high and steep impurity profile

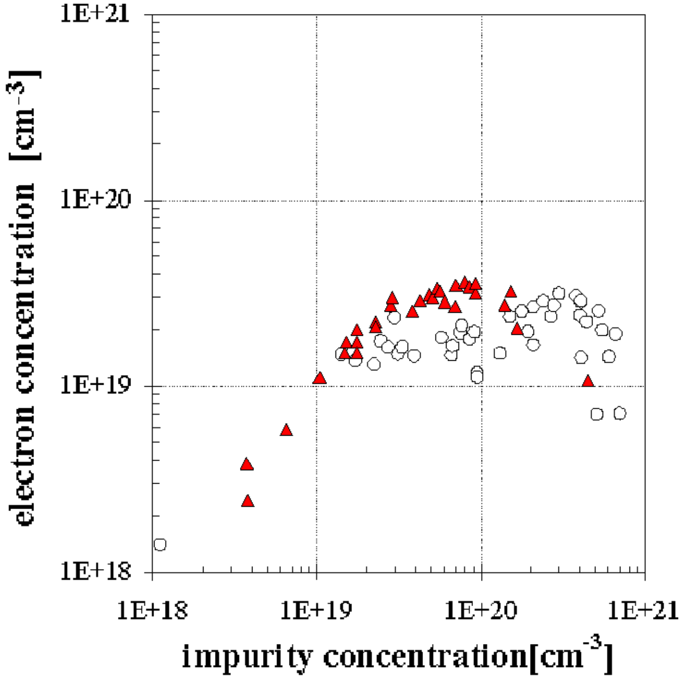


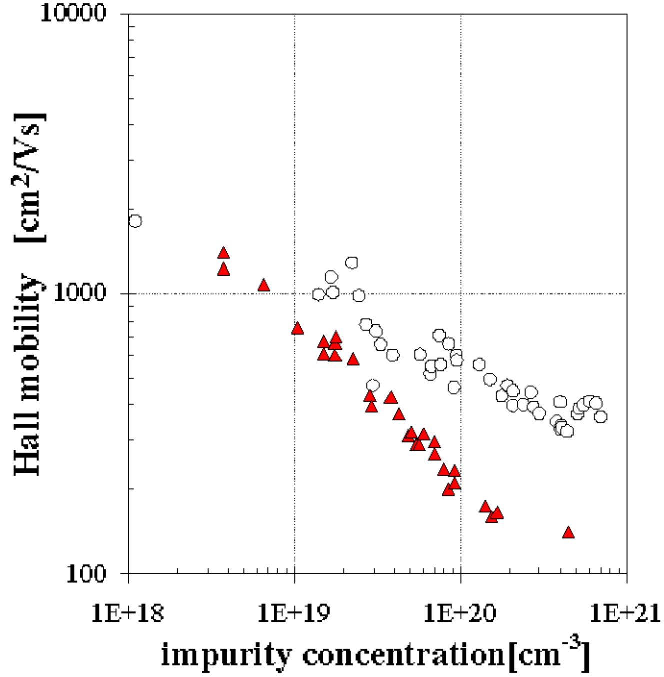
Doping mode dependences of impurity concentration evaluated by one-epitaxial run: base DETe doping.





DOPING CHARACTERISTICS OF n-GaAs MLE





▲Te DOPING

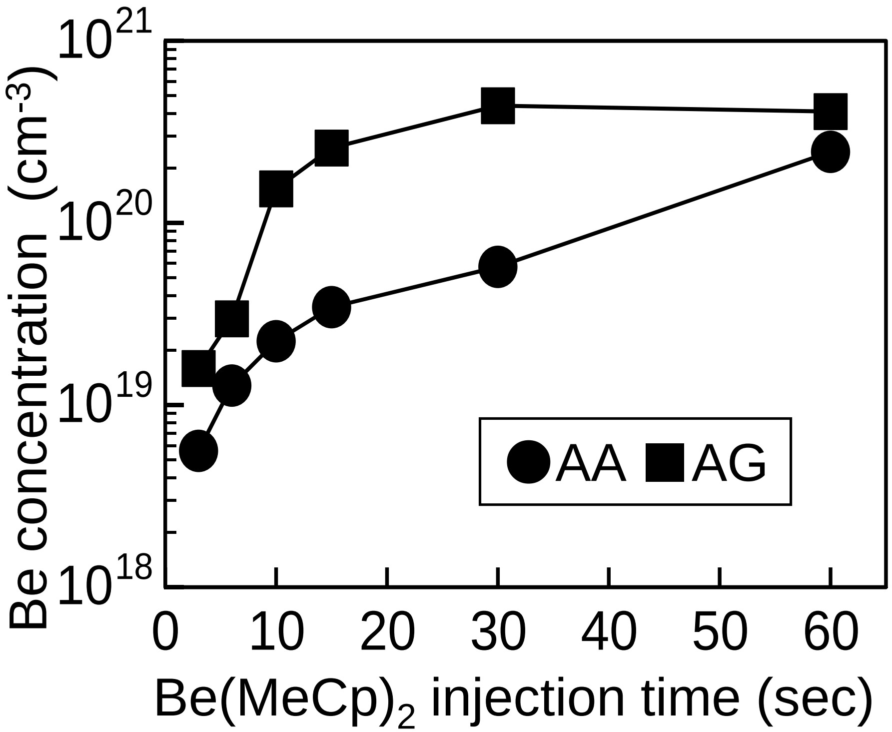
○Se DOPING

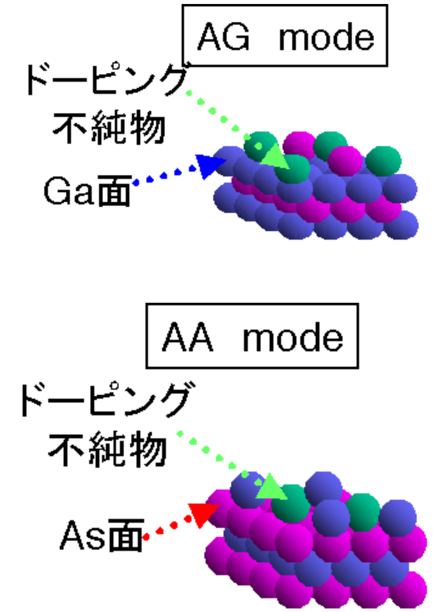
UP TO 10^{21}cm^{-3} IMPURITY CONCENTRATION

5×10^{19}cm^{-3} ELECTRON CONCENTRATION

Required for nm-channel Tr.

DOPING CHARACTERISTICS OF p-GaAs:Be MLE





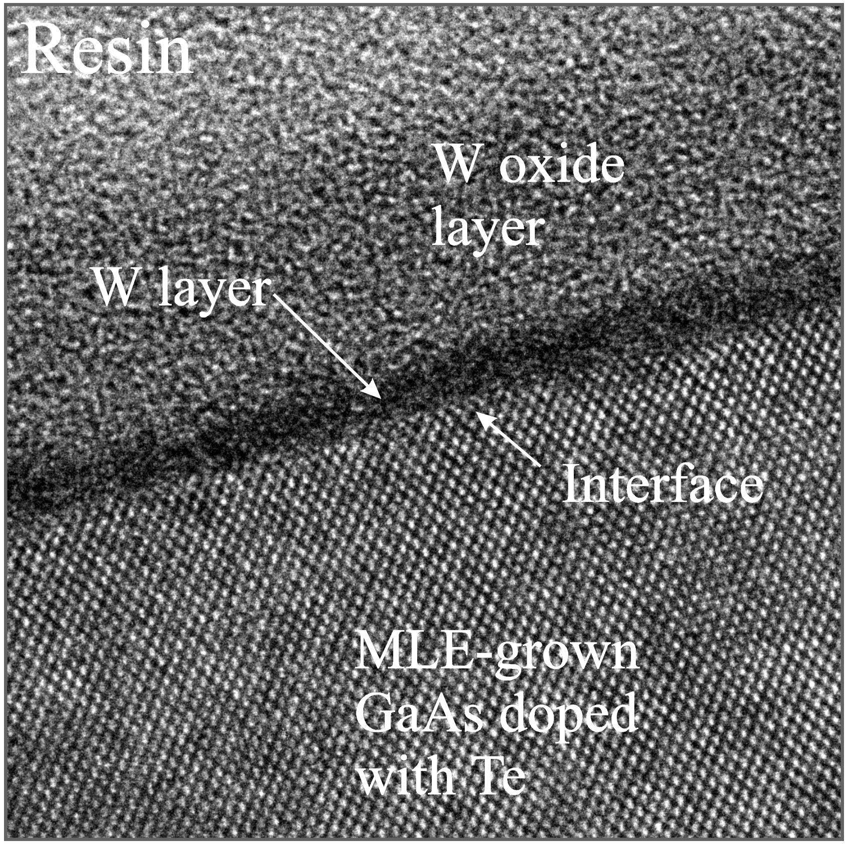
Ohno T et. al.

UP TO $4x10^{20}cm^{-3}$ IMPURITY CONCENTRATION

$8x10^{19}cm^{-3}$ HOLE CONCENTRATION

Required for nm-channel Tr.

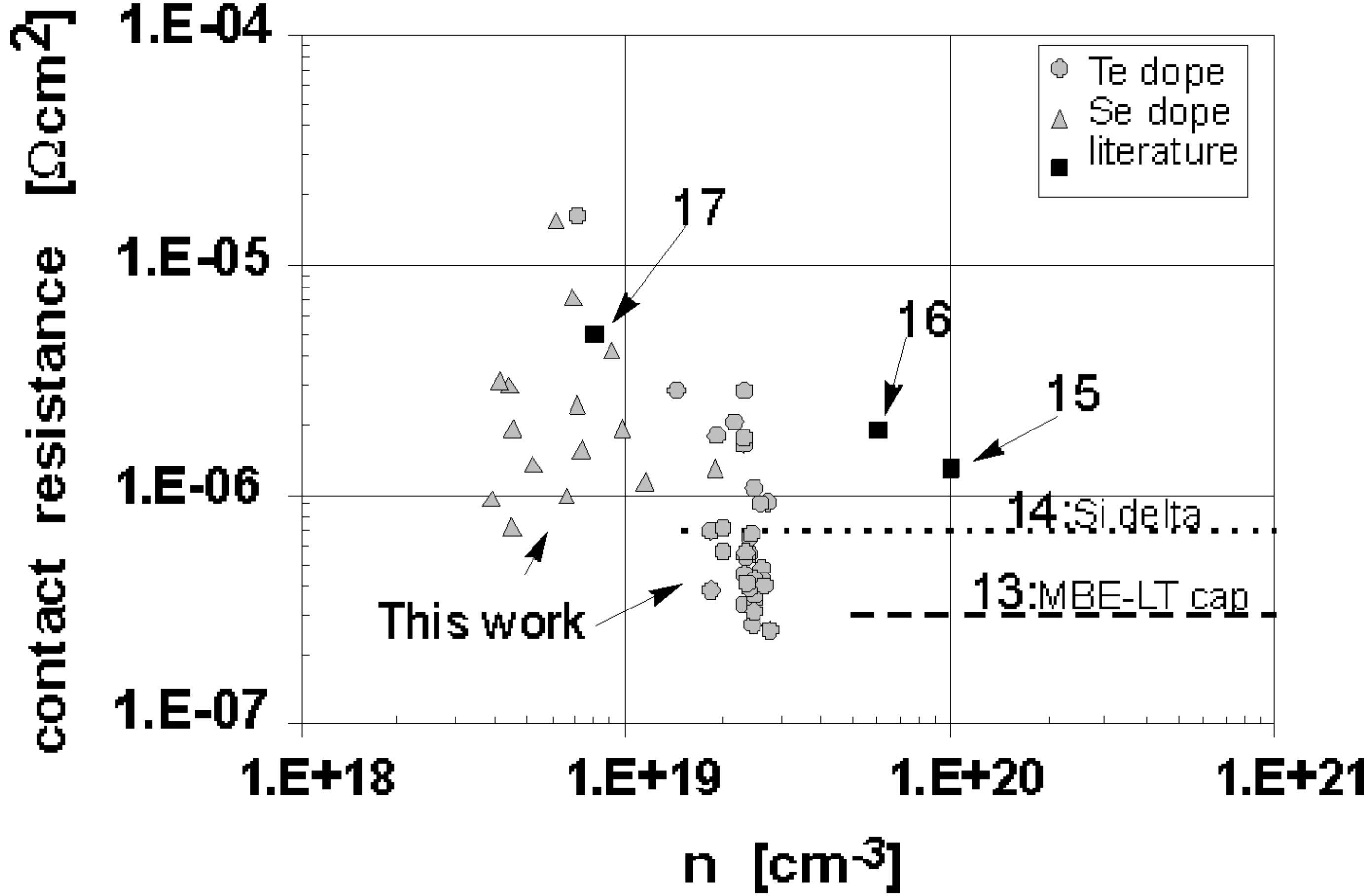
Ultra low ρ_c metal/semiconductor contact: non-alloyed and selective CVD by $W(CO)_6$



XTEM of MS interface with atomically flat interface

Low-resistance Contacts with Chemical Vapor Deposited Tungsten on GaAs Grown by Molecular Layer Epitaxy
[J. Electrochem. Soc., 146 (1), (1999), 131 - 136]
Yutaka Oyama, Piotr Plotka, Fumio Matsumoto, Toru Kurabayashi, H.hamano, Hideyuki Kikuchi and Jun-ichi Nishizawa など

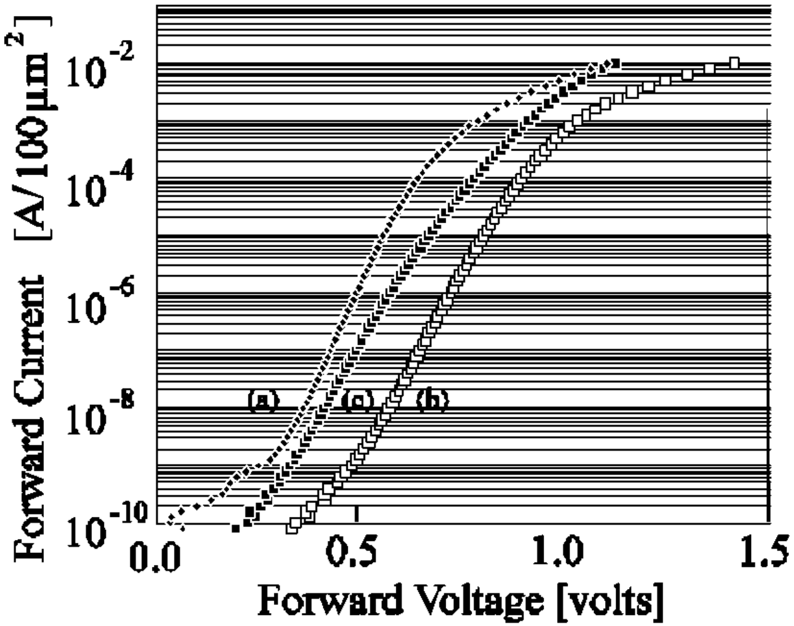
Contact resistivity for n-GaAs (MLE grown)

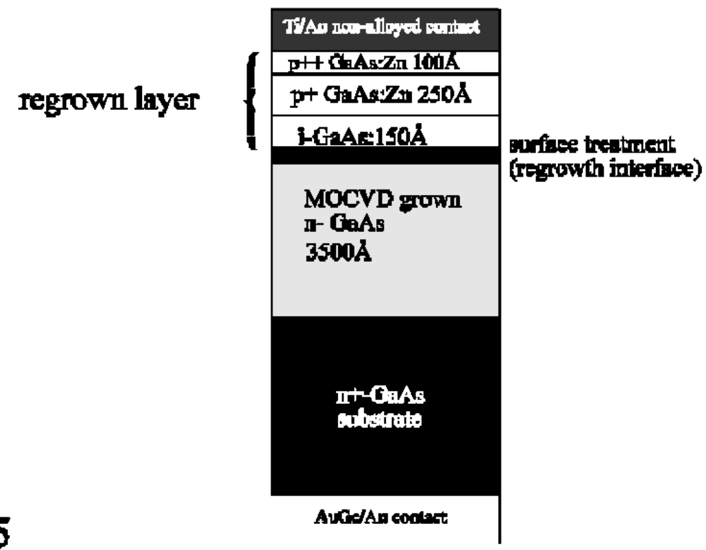


Also for *p*-GaAs (down to $10^{-8}\Omega cm^2$ order)
Almost the limit of TLM method

High quality regrown interface

Good interface →

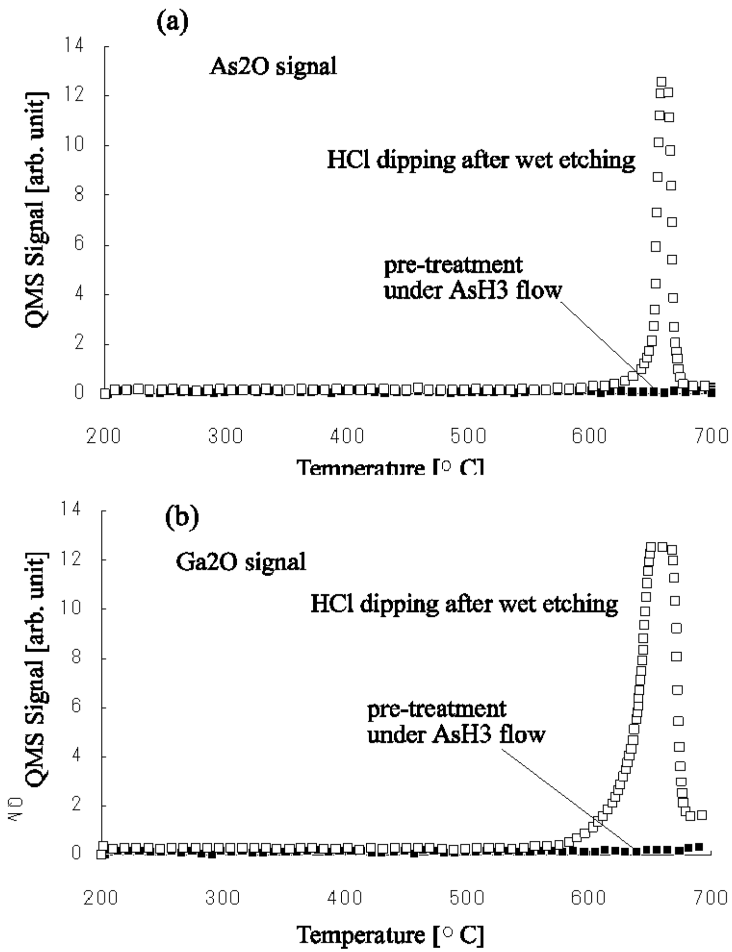




Structure of
regrown pin diode

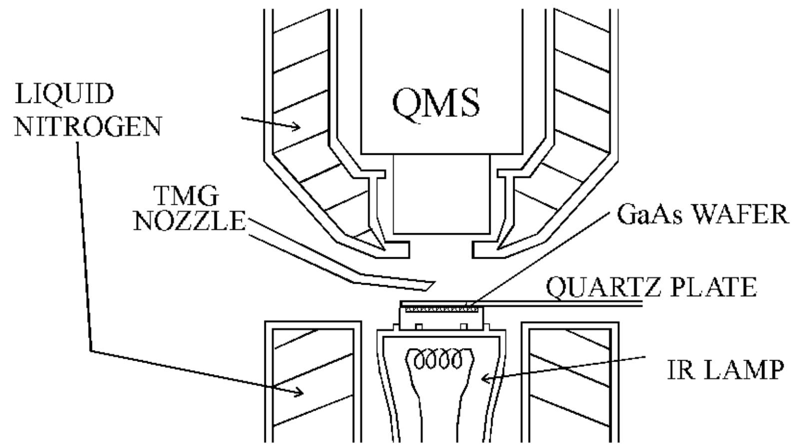
"Optimization of low temperature surface treatment of GaAs crystal",
J.Nishizawa, Y.Oyama, P.Plotka and H.Sakuraba,
Surface Science, 348, 105-114 (1996). など

High quality regrown interface: chemical analysis



No trace of oxides and carbide after optimized surface treatment
QMS desorption analysis

Also by XPS analysis



Application of MLE GaAs to high quality ultra-small tunnel junctions
Side-wall regrowth process

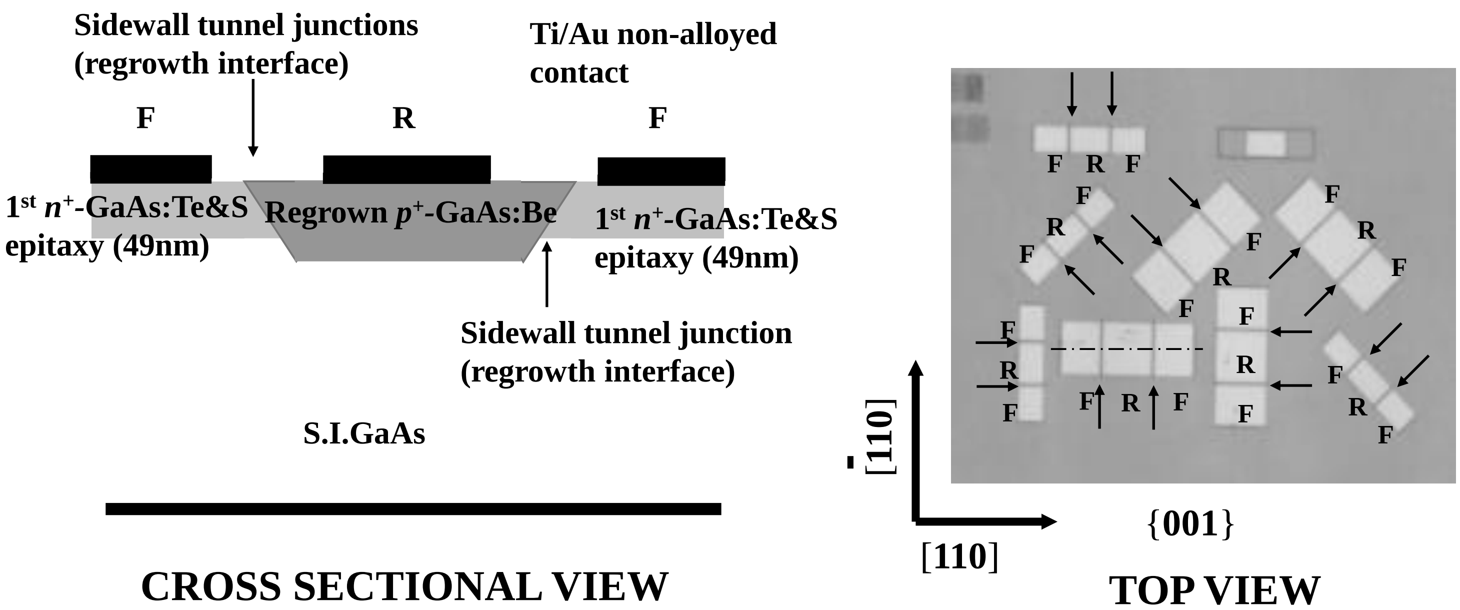
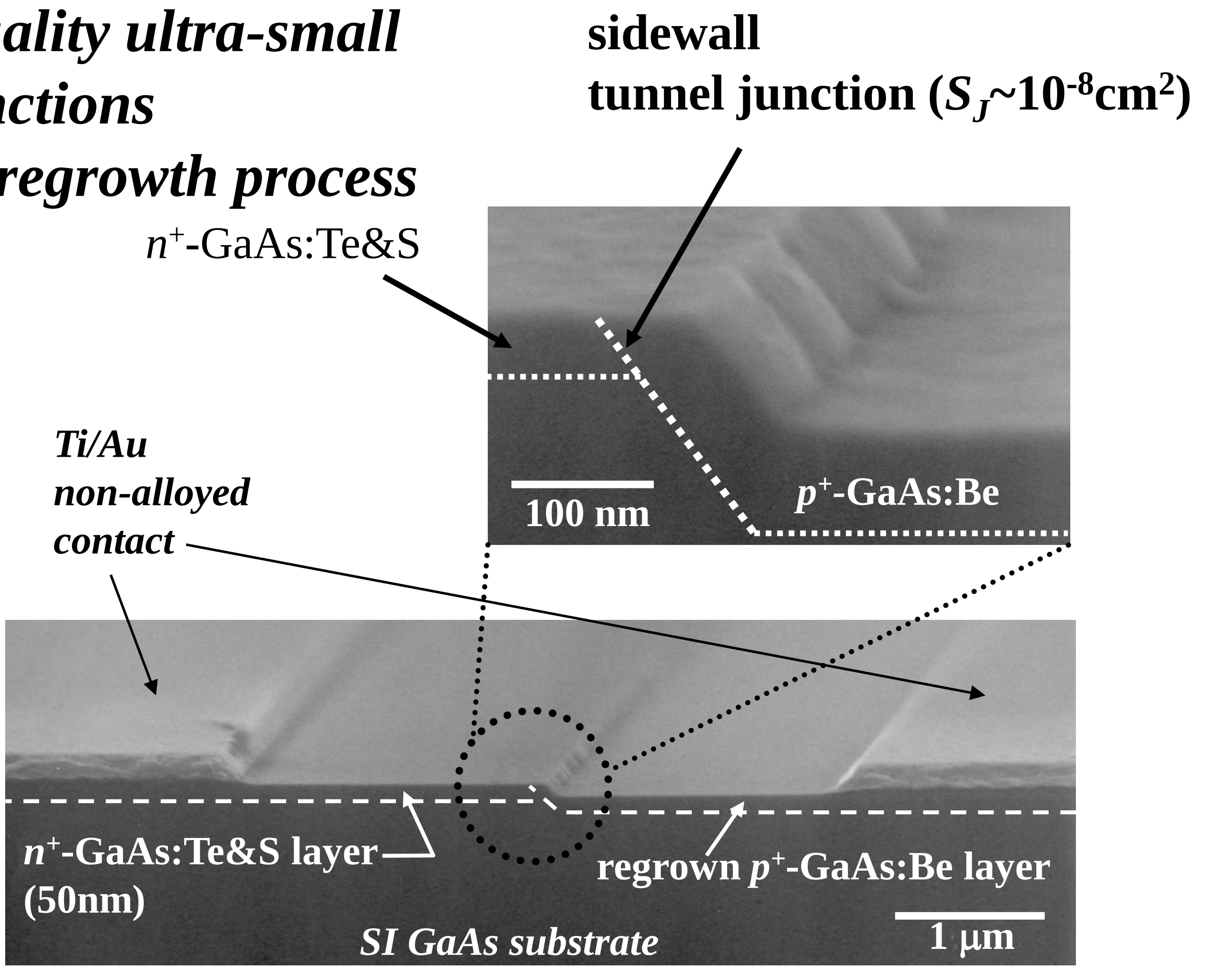


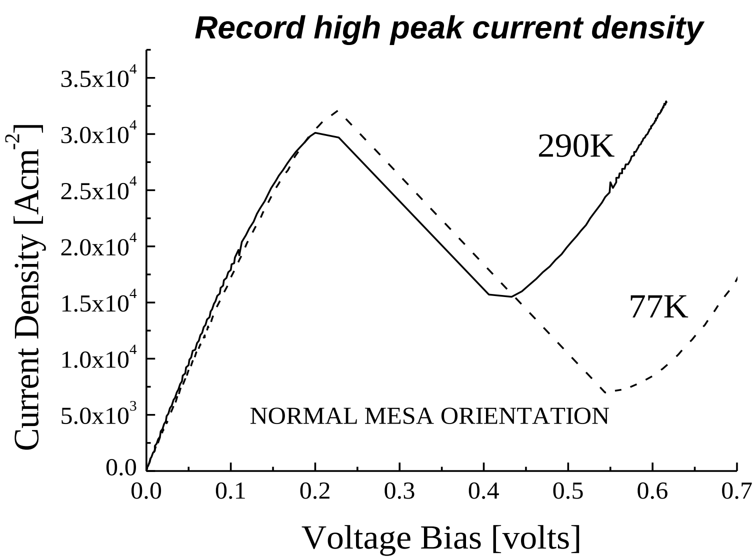
Figure 1. Schematic drawings of the cross sectional and top view of the fabricated sidewall tunnel diodes. "F" and "R" mean the first epitaxial layers and the regrowth layers. The arrows indicate the positions of sidewall regrown tunnel junctions. Large pad has 100 μm in length, and small one has 50 μm.

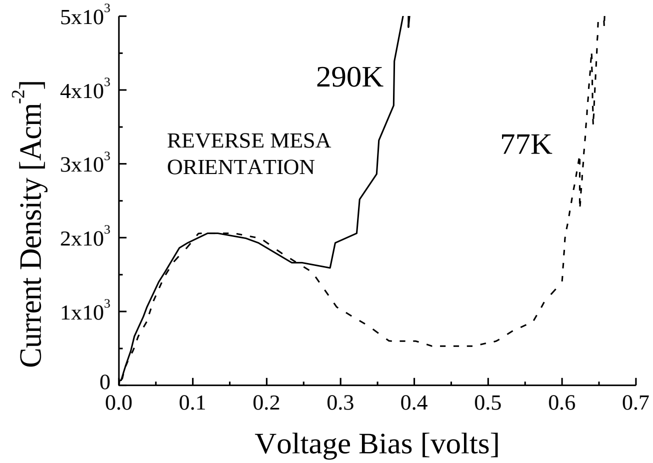
Application of low-temperature area-selective regrowth for ultrashallow sidewall GaAs tunnel junctions
Yutaka Oyama, Takeo Ohno, Kenji Tezuka, Ken Suto and Jun-ichi Nishizawa
Applied Physics Letters, 81, 2563-2565 (2002). など

Application of MLE GaAs to high quality ultra-small tunnel junctions
Side-wall regrowth process



Current-voltage characteristics of sidewall TUNNEL junctions
Sidewall mesa orientation dependences





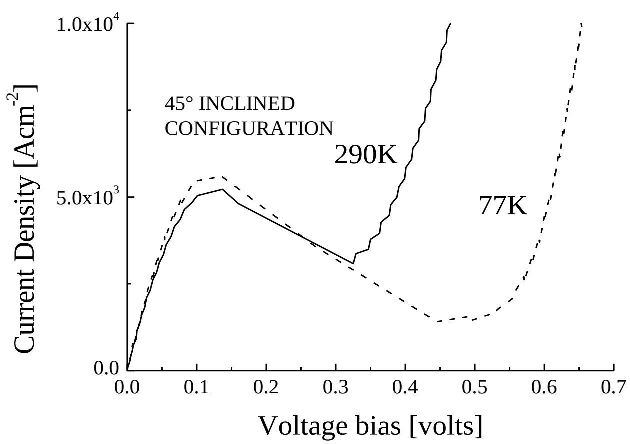
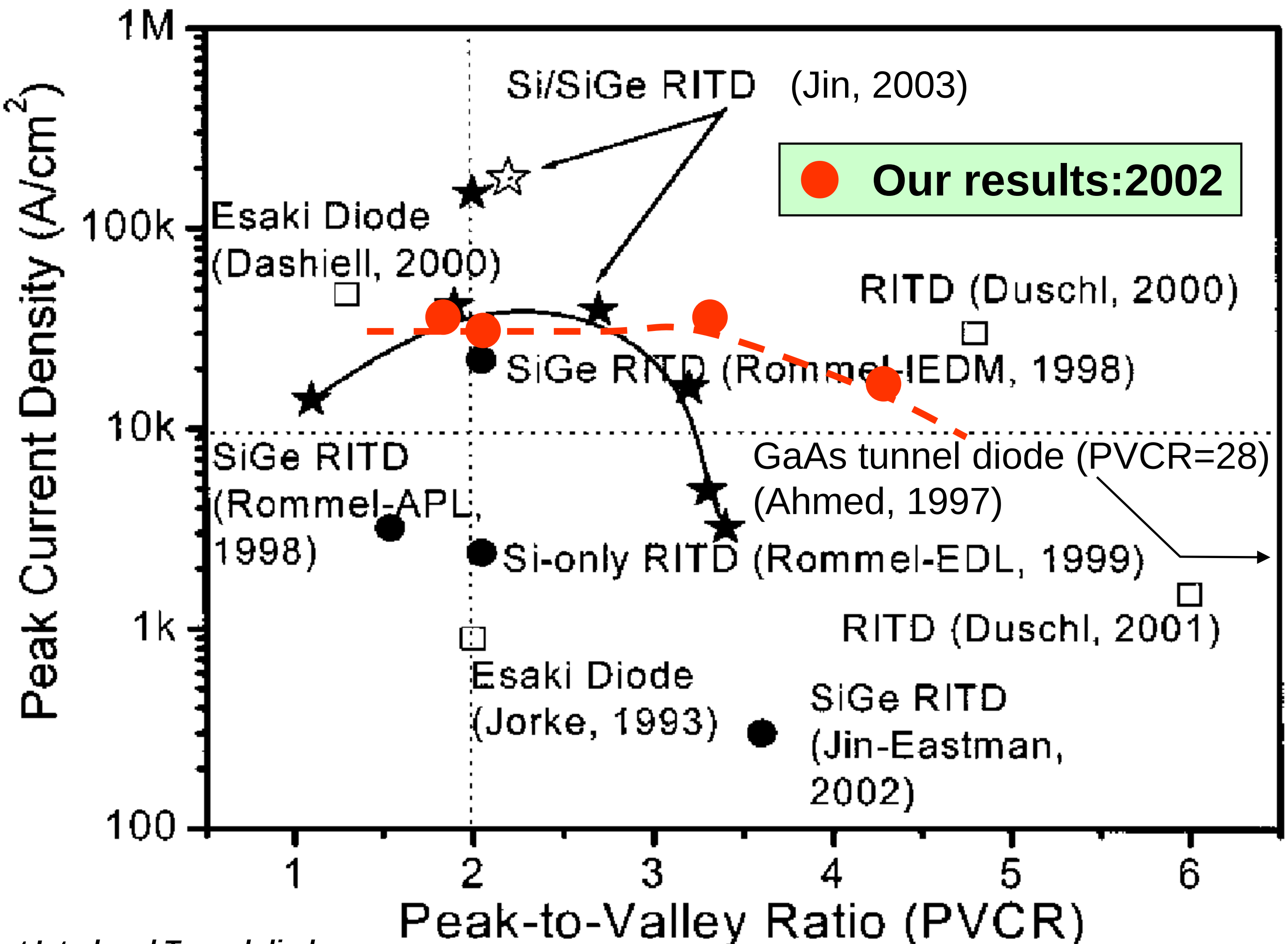


Figure 2. J-V characteristics of GaAs sidewall tunnel junctions at 290 and 77K on (a) normal mesa, (b) 45° inclined configuration and (c) reverse mesa sidewall orientations.

Ohno T et. al.

Figure of merits of fabricated TUNNEL junctions



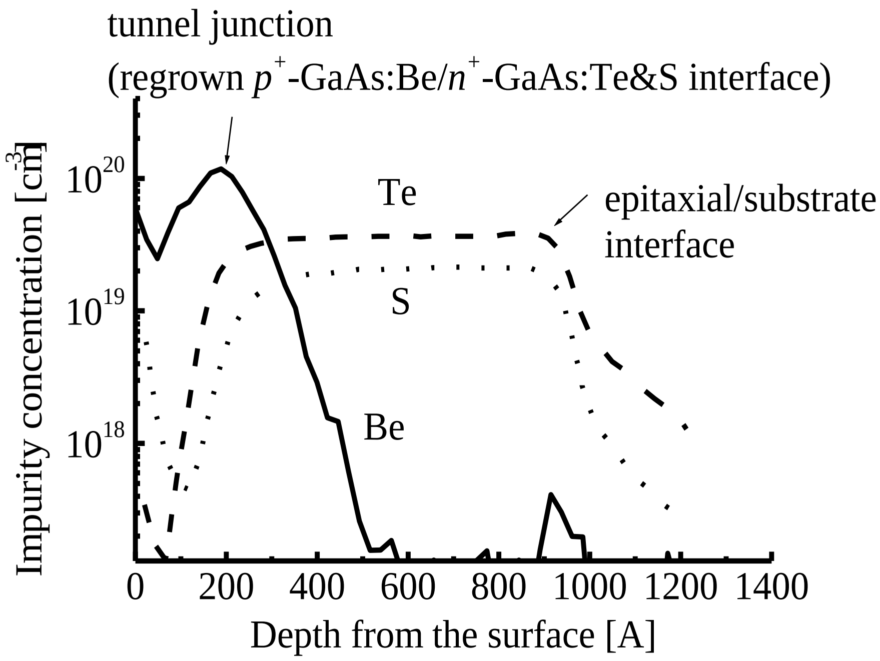
RITD:
Resonant Interband Tunnel diode

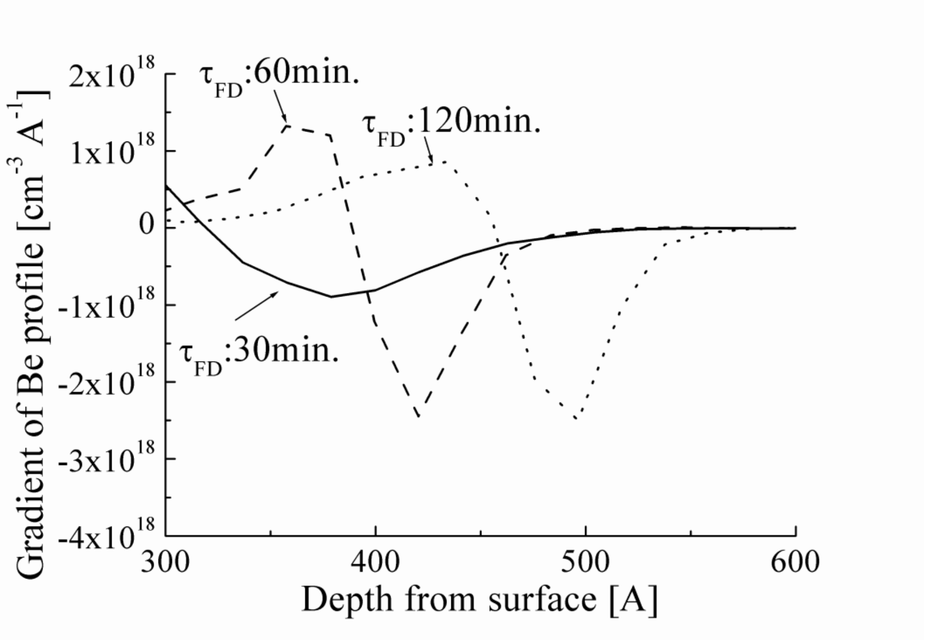
Ohno T et. al.

Very high & steep impurity profile at tunnel junction interface

up to 2x10^18 cm^-3 impurities /A

Ohno T et. al.





To be continued to next week

Ultra fast and high frequency semiconductor electronic and photonic devices